ATP SATA3 mSATA Embedded Module Specification

Version 1.0

ATP Electronics, Inc.

CONTENT

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Revision History

Date	Version	Revision History
Jan. 12th , 2016	1.0	- New BOM Release

1.0 ATP mSATA Embedded Module Overview

1.1 ATP Product Image

Figure 1-1: ATP Product Image (reference only)

Table 1-1: Capacities

ATP P/N	CAPACITY
AF16GSMHI-VADXP	16GB
AF32GSMHI-VADXP	32GB
AF64GSMHI-VACXP	64GB
AF128GSMHI-VACXP	128GB
AF256GSMHI-VAAXP	256GB
AF512GSMHI-VAAXP	512GB

Note: GB = 1,000,000,000 Byte

1.2 Introduction

The ATP mSATA Embedded Module is a high performance and high capacity mass storage solution in Slim form factor. Utilizing MLC (Multi-Level Cell) NAND Flash components provides outstanding performance and proven reliability for products operating.

ATP mSATA Embedded Module is perfect for thin devices, especially networking, thin clients, embedded appliance, and also suitable for industrial applications such as transportation, industrial PC, healthcare, telecommunications, and other harsh environments where data integrity and consistent performance is mission critical.

1.3 Main Features

- Capacity: 16GB~512GB
- MLC (Multi-Level Cell) NAND flash memory
- Operating temperature: 0℃ to 70℃
- Maximum performance: Sequential read up to 530 MB/s, sequential write up to 440 MB/s
- JEDEC standard: MO-300A
- Compliant with Serial ATA Revision 3.2
- SATA 6.0Gbps interface and backward compatible with 1.5Gbps and SATA 3Gbps interface rate
- Hardware BCH ECC, correct up to 60-bit ECC per 1024 bytes of data
- SMART function support by ATA CMD
- Enhanced endurance by Global wear-leveling
- AutoRefresh, automatic data protection in read operation
- PowerProtector Gen.2, data integrity under power-cycling
- CE, FCC certification

PowerProtector – Power Cycling Protection

The unstable power conditions of outdoor applications such as transportation, telecommunications/networking and embedded systems run the risk of data loss and drive corruption during a sudden power failure.

A standalone hardware design is the ideal configuration for power backup, ensuring a sufficient amount of reserve power during any power abnormalities and minimizing the consequent host re-designs for adding new features. During a sudden power failure, the abnormality is discovered by a power loss detection circuit and activates the power protection mechanism. The device then draws power from power protection reservoir, where the reserve power is stored. The reserve power gives enough time for the flash device to conclude the last writing command without losing any data.

AutoRefresh Technology – Data Integrity Protection

Over time the error bits accumulate to the threshold in the flash memory cell and eventually become uncorrectable despite using the ECC engine. In the traditional handling method, the data is moved to a different location in the flash memory; despite the corrupted data is beyond repaired before the transition.

The situation is worse in frequent read applications, such as navigation systems or OS boot-up devices. The map or operation system is preloaded into the storage media and there may be one time write and following by read operation only. Read disturbance is the result of electrical interference from multiple read operations in surrounding pages. After NAND flash accumulates 100,000 read cycles, uncorrectable ECC errors may occur in the affected pages which results in data failure in the same block.

To prevent data corruption, ATP memory product monitors the error bit levels in each read operation; when it reaches the preset threshold value, AutoRefresh is activated by programming the data into another block before the data is corrupted. After the re-programming operation is completed, the controller reads the data and compares the data/parity to ensure data integrity.

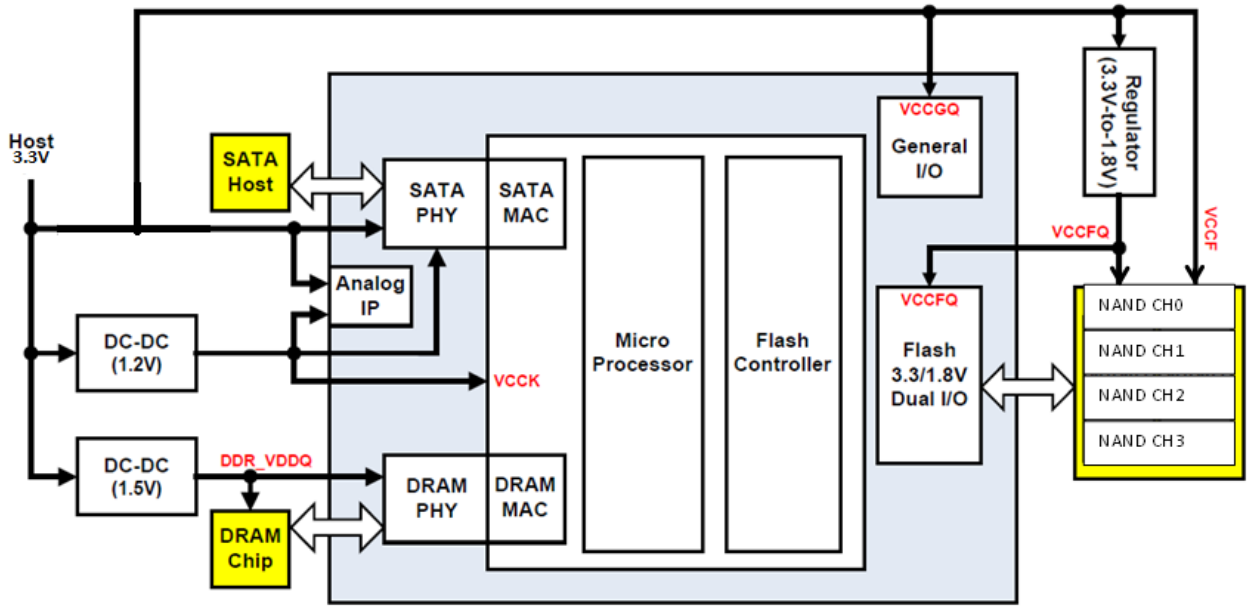
Owing to different user experiences, please contact ATP for AutoRefresh in real applications.

2.0 Product Specification

2.1 Block Diagram

ATP mSATA Embedded Module consists of below functional blocks. The advanced architecture is optimized to provide highest data reliability and transfer performance.

Figure 2-1:



2.2 Environment Specifications

Table 2-1

Type		Standard
Temperature	Operating	0°C to 70°C
	Non-Operating	-40°C to 85°C
Humidity	Operating	25°C, 8% to 95%, noncondensing
	Non-Operating	40°C, 8% to 93%, noncondensing
Vibration	Non-Operating	sine 16.4G, 10~2000Hz
Shock	Non-Operating	Half sine 1500G/0.5ms
Altitude	Operating	80,000 feet Max.
	Non-Operating	80,000 feet Max.

2.3 IOPS Performance

Table 2-2

Type	Value
4K Random Read IOPS	Up to 72,040 IOPS

Note: Input/Output operations per second tested by Crystal Disk Mark on 512GB device.

2.4 Maximum Read/Write Performance

Table 2-3

Type		16GB	32GB	64GB	128GB	256GB	512GB
Crystal Disk Mark	Sequential Read (MB/s)	110	220	400	520	520	530
	Sequential Write(MB/s)	20	40	75	130	260	440

2.5 Electrical Characteristics

Table 2-4

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Supply voltage	V_{CC}	3.15	3.3	3.45	V	

Table2-5

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Sustained write power	P_W	0.50	3.80	5.65	W	RMS value
Sustained read power	P_R	0.50	1.65	2.75	W	RMS value
Idle power	P_S	0.30	0.35	0.45	W	RMS value

2.6 Reliability

Table2-6

Type	Value
MTBF (@ 25°C) [1]	2,000,000 hours
Data Retention (@ 55°C)	5 years (with 10% P/E cycle)

Notes: The Mean Time between Failures (MTBF) is calculated using a prediction methodology, Telcordia SR-332, which based on reliability data of the individual components in the mSATA. It assumes nominal voltage, with all other parameters within specified range.

2.7 Write/Erase Endurance[1]

Table 2-7

Type	Value
Endurance Technology	Enhanced global dynamic and static wear-leveling algorithm MLC Flash block: 3,000 P/E cycles
SSD Endurance	16GB: 6.85 TB Random write 19.2 TB Sequential write 32GB: 13.71 TB Random write 38.4 TB Sequential write 64GB: 27.43 TB Random write 76.8 TB Sequential write 128GB: 54.86 TB Random write 153.6 TB Sequential write 256GB: 109.7 TB Random write 307.2 TB Sequential write 512GB: 219.43 TB Random write 614.4 TB Sequential write

Note:

1. Endurance for the mSATA can be predicted based on the usage conditions applied to the device, the internal NAND component cycles, the write amplification factor, and the wear leveling efficiency of the drive. TBW may vary depending on application, please contact ATP for TCO evaluation if specific usage type applies.
2. The random endurance is based on JEDEC219 enterprise workload.

2.8 Certification and compliance

Table 2-9

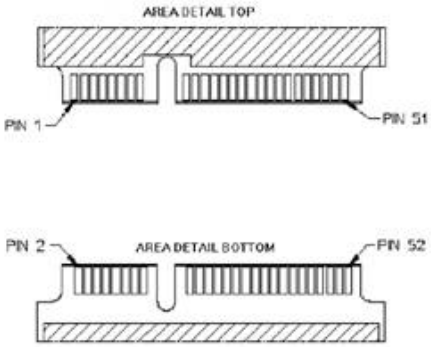
Mark/Approval	Documentation	Certification
CE	The CE marking (also known as CE mark) is a mandatory conformance mark on many products placed on the single market in the European Economic Area (EEA). The CE marking certifies that a product has met EU consumer safety, health or environmental requirements. CE stands for Conformité Européenne, "European conformity" in French.	Yes
FC	FCC Part 15 Class B was used for Evolution of United States (US) Emission Standards for Commercial Electronic Products, The United States (US) covers all types of unintentional radiators under Subparts A and B (Sections 15.1 through 15.199) of FCC 47 CFR Part 15, usually called just FCC Part 15	Yes

3.0 SATA SSD Pin Assignment

3.1 Pin Location

The following figure shows the pin location of the mSATA, the connector is with both signal and power segments.

Figure 3-1



3.2 Pin Assignment

There are total of 52 pin and the pin definitions are shown in Table 3-1

Table 3-1

Pin No.	Function	Description
P1	Reserved	No Connect
P2	+3.3V	3.3V Source
P3	Reserved	No Connect
P4	GND	Return Current Path
P5	Reserved	No Connect
P6	+1.5V	Not used in ATP design
P7	Reserved	No Connect
P8	Reserved	No Connect
P9	GND	Return Current Path
P10	Reserved	No Connect
P11	Reserved	No Connect
P12	Reserved	No Connect
P13	Reserved	No Connect
P14	Reserved	No Connect
P15	GND	Return Current Path
P16	Reserved	No Connect
P17	Reserved	No Connect
P18	GND	Return Current Path
P19	Reserved	No Connect

Pin No.	Function	Description
P20	Reserved	No Connect
P21	GND	Return Current Path
P22	Reserved	No Connect
P23	+B	Host Receiver Differential Signal Pair
P24	+3.3V	3.3V Source
P25	-B	Host Receiver Differential Signal Pair
P26	GND	Return Current Path
P27	GND	Return Current Path
P28	+1.5V	Not used in ATP design
P29	GND	Return Current Path
P30	Two Wire Interface	Two Wire interface Clock[3]
P31	-A	Host Transmitter Differential Signal Pair
P32	Two Wire Interface	Two Wire interface Data[3]
P33	+A	Host Transmitter Differential Signal Pair
P34	GND	Return Current Path
P35	GND	Return Current Path
P36	Reserved	No Connect
P37	GND	Return Current Path
P38	Reserved	No Connect
P39	+3.3V	3.3V Source
P40	GND	Return Current Path
P41	+3.3V	3.3V Source
P42	Reserved	No Connect
P43	Reserved	Shall be a No Connect on mSATA Devices[4]
P44	Reserved	Enter/Exit DevSleep
P45	Vender	Not used in ATP design [2]
P46	Reserved	No Connect
P47	Vender	Not used in ATP design [2]
P48	+1.5V	Not used in ATP design
P49	DAS/DSS	Device Activity Signal / Disable Staggered Spin-up
P50	GND	Return Current Path
P51	Presence Detection	Shall be pulled to GND by a 0 ohm to 220 ohm resistor on device[1]
P52	+3.3V	3.3V Source

Notes:

1. Presence detection pin indicates presence of an mSATA device.

2. No connect on the host side.

3. Pins 30 and 32 are intended for use as a two wire interface to read a memory device to determine device information (an example of this would be for use as SMB bus pins). These pins are not designed to be active in conjunction with the SATA signal differential pairs. Not used in ATP design.

4. P43 to be a no connect on mSATA devices. Given that non-mSATA devices ground P43, configurable shared-socket designs may use this pin to identify mSATA and non-mSATA devices.

4.0 Command Set

4.1 ATA Command Set

ATP mSATA support the commands show in the following table

Table 4-1

Command	Code	Protocol
General Feature Set		
Execute Drive Diagnostic	90h	Device diagnostic
Flush Cache	E7h	Non-data
Flush Cache Ext	EAh	Non-data
Identify Device	ECh	PIO data-in
Initialize Drive Parameters	91h	Non-data
Read DMA	C8h	DMA
Read DMA Ext	25h	DMA
Read Log Ext	2Fh	PIO data-in
Read Multiple	C4h	PIO data-in
Read Sector(s)	20h or 21h	PIO data-in
Read Sector(s) Ext	24h	PIO data-in
Read Verify Sector(s)	40h or 41h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Feature	EFh	Non-data
Set Multiple Mode	C6h	Non-data
Write DMA	CAh	DMA
Write DMA Ext	35h	DMA
Write DMA Fua Ext	3Dh	DMA
Write Log Ext	3Fh	PIO data-out
Write Multiple	C5h	PIO data-out
Write Sector(s)	30h or 31h	PIO data-out
Write Sector(s) Ext	34h	PIO data-out

NOP	00h	Non-data
Read Buffer	E4h	PIO data-in
Write Buffer	E8h	PIO data-out
Data Set Management Download Microcode	06h 92h	DMA PIO data-out
Power Management Feature Set		
Check Power Mode	E5h or 98h	Non-data
Idle	E3h or 97h	Non-data
Idle Immediate	E1h or 95h	Non-data
Sleep	E6h or 99h	Non-data
Standby	E2h or 96h	Non-data
Standby Immediate	E0h or 94h	Non-data
Security Mode Feature Set		
Security Set Password	F1h	PIO data-out
Security Unlock	F2h	PIO data-out
Security Erase Prepare	F3h	Non-data
Security Erase Unit	F4h	PIO data-out
Security Freeze Lock	F5h	Non-data
Security Disable Password	F6h	PIO data-out
SMART Feature Set		
SMART Disable Operation	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Return Status	B0h	Non-data
SMART Execute Off-Line Immediate	B0h	Non-data
SMART Read Data	B0h	PIO data-in
SMART Read Threshold	B0h	PIO data-in
SMART Read Log	B0h	PIO data-in
SMART Write Log	B0h	PIO data-out
SMART Save Attribute Values	B0h	Non-data
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Read Native Max Address Ext	27h	Non-data
Set Max Address	F9h	Non-data
Set Max Address Ext	37h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data

Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out

4.2 Identity Device Data

Table 4-2

Word Address	Default Value	Data Field Type Information
0	0040h	General Configuration
1	XXXXh	Default number of cylinders
2	0000h	Reserved
3	00XXh	Default number of heads
4	0000h	Obsolete
5	0240h	Obsolete
6	XXXXh	Default number of sectors per track
7-8	XXXXh	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	Obsolete
10-19	XXXXh	Serial number in ASCII (Left justified) with 12 or less characters
20	0002h	Obsolete
21	0002h	Obsolete
22	0000h	Obsolete
23-26	XXXXh	Firmware revision in ASCII (Left justified). Big Endian Byte Order in Word
27-41	XXXXh	Model number in ASCII (Left justified). Big Endian Byte Order in Word
42~46		Part number in ASCII (Right justified) preceded by the ANSI space character
47	8001h	Maximum number of sectors on Read/Write Multiple command
48	0000h	Reserved
49	0F00h	Capabilities
50	4000h	Capabilities
51	0200h	PIO data transfer cycle timing mode
52	0000h	Obsolete
53	0007h	Field validity
54	XXXXh	Current numbers of cylinders
55	XXXXh	Current numbers of heads
56	XXXXh	Current sectors per track

57-58	XXXXh	Current capacity in sectors (LBAs) (Word57=LSW, Word58=MSW)
59	0101h	Multiple sector setting
60-61	XXXXh	Total number of user addressable logical sectors for 28-bit commands (DWord)
62	0000h	Reserved
63	0207h	Multiword DMA transfer Supports MDMA Mode 0, 1, and 2
64	0003h	Advanced PIO modes supported
65	0078h	Minimum Multiword DMA transfer cycle time per word
66	0078h	Recommended Multiword DMA transfer cycle time
67	0078h	Minimum PIO transfer cycle time without flow control
68	0078h	Minimum PIO transfer cycle time with lORDY flow control
69	4000h	Additional supported
70~74	0000h	Reserved
75	0031	Queue depth
76	030E	Serial ATA capabilities Support Serial ATA Gen1 Support Serial ATA Gen2 Support Serial ATA Gen3 Supports Phy event counters log Support receipt of host-initiated interface power management requests Supports Native Command Queuing
77	0080h	Serial ATA additional capability DevSleep_to_ReducedPwerState
78	044C	Serial ATA features supported Supports Device Sleep Supports software settings preservation Device supports initiating power management
79	0040h	Reserved
80	03F0h	Major version number (ACS-2)
81	0000h	Minor version number
82	742Bh	Command sets supported 0
83	7500h	Command sets supported 1
84	4023h	Command sets supported 2
85~87	XXXXh	Command set/feature enabled
88	007Fh	Ultra DMA supported and selected

89	0003h	Time required for Normal Erase mode Security Erase Unit command
90	0001h	Time required for Enhanced Erase mode Security Erase Unit command
91	0000h	Current advanced power management value
92	FFFEh	Master password identifier
93~99	0000h	Reserved
100~103	XXXXh	Maximum user LBA for 48-bit address feature set
104	0000h	Reserved
105	0100h	Maximum number of 512-byte blocks per Data Set Management command
106	5000	bit 12 = 1 to indicate that the Logical Sector Size field is valid
		Bit 14 = 1
		Bit 15 = 0
107~116	0000h	Reserved
117~118	0x800	Logical sector size
119~127	0000h	Reserved
128	0001h	Security status
129~159	XXXXh	Vendor specific
160	0000h	Power requirement description
161	0000h	Reserved
162	0000h	Key management schemes supported
163	0000h	CF Advanced True lDE Timing Mode Capability and Setting
164~168	0000h	Reserved
169	0001h	Data Set Management supported
170~216	XXXXh	Reserved
217	0001h	Non-rotating media(SSD)
218~221	0000h	Reserved
222	107Fh	Transport major revision (SATA Rev 3.1)
223~254	0000h	Reserved
255	XXXXh	Integrity word

4.3 Smart Information

ATP mSATA supports S.M.A.R.T. ATA feature set in IDE mode, AHCI mode, not support in RAID mode.

4.3.1 Smart Subcommand Sets

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the SMART Function Set command. The subcommands are listed below.

Table 4-3

Command	Command Code
SMART READ DATA	D0h
SMART READ ATTRIBUTE THRESHOLD	D1h
SMART ENABLE/DISABLE AUTOSAVE	D2h
SMART SAVE ATTRIBUTE VALUES	D3h
SMART EXECUTE OFF-LINE IMMIDIATE	D4h
READ LOG	D5h
WRITE LOG	D6h
SMART ENABLE OPERATIONS	D8h
SMART DISABLE OPERATIONS	D9h
SMART RETURN STATUS	DAh

Note: If the reserved size is below a threshold, status can be read from the Cylinder Register using the Return Status command (DAh)

4.3.2 SMART Read Data (Subcommand Doh)

The following 512 bytes make up the device SMART data structure. Users can obtain the data using the “Read Data” command (D0h).

Table 4-4

Byte	F/V	Description
0~1	X	Revision code
2~361	X	Vendor Specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364~365	V	Total time in seconds to complete off-line data collection activity

366	X	Vendor Specific
367	F	Off-line data collection capability
368~369	F	SMART capability
370	F	Error logging capability: 7-1 = Reserved 0 -1 = Device error logging supported
371	X	Vendor Specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375~385	R	Reserved
386~395	F	Firmware Version/Date Code
396~397	F	Reserved
398~399	F	Reserved
400~408	F	SMI2246EN
409~415	X	Vendor specific
416	F	Reserved
417	F	Program/write the strong page only
418~419	V	Number of spare block
420~423	V	Average erase count
424~510	X	Vendor Specific
511	V	Data structure checksum

Notes:

1. F=content (byte) is fixed and does not change
2. V=content (byte) is variable and maybe change depending on the state of the device or the command executed by the device
3. X= content (byte) is vendor specific and maybe fixed or variable
4. R=content (byte) is reserved and shall be zero

4.3.3 SMART Attribute

The following table defines the vendor specific data in byte 2 to 361 of the 512-byte SMART data.

Table 4-5

ID	Value (hex)	Raw Attribute Value							Attribute Name
1	01	LSB	MSB	0	0	0	0	0	Raw Read Error Count (0x01)
5	05	LSB	MSB	0	0	0	0	0	Reallocated Sectors Count
9	09	LSB			MSB	0	0	0	Power On Hours (0x09)
12	0C	LSB			MSB	0	0	0	Normal Power On/Off count
14	0E	LSB			MSB	0	0	0	Device Physical Capacity (0x0E)
15	0F	LSB			MSB	0	0		Device User Capacity (0x0F)
16	10	LSB	MSB	0	0	0	0	0	Initial Spare blocks (0x10)
17	11	LSB	MSB	0	0	0	0	0	Remaining Spare Blocks at Current Time (0x11)
100	64	LSB			MSB	0	0	0	Total Erase Count
160	A0	LSB			MSB	0	0	0	Uncorrectable Sector Count When Read/Write
172	AC	LSB	MSB	0	0	0	0	0	Total Block Erase Failure (0xAC)
173	AD	LSB			MSB	0	0	0	Maximum Erase Count (0xAD)
174	AE	LSB			MSB	0	0	0	Unexpected Power Loss Count
175	AF	LSB			MSB	0	0	0	Average Erase Count
181	B5	LSB			MSB	0	0	0	Total Block Program Failure

ID	Value (hex)	Raw Attribute Value							Attribute Name
187	BB	LSB			MSB	0	0	0	Reported Uncorrectable Errors (0xBB)
194	C2	LSB MSB	0	0	0	0	0	0	Device Temperature (0xC2)
195	C3	LSB			MSB	0	0	0	Hardware ECC Recovered
197	C5	LSB MSB	0	0	0	0	0	0	Current Pending Block Count (0xC5)
198	C6	LSB			MSB	0	0	0	Offline Surface Scan (0xC6)
199	C7	LSB	MSB	0	0	0	0	0	SATA FIS CRC Errors
202	CA	LSB			MSB	0	0	0	Percentage of Drive Life Used
205	CD	LSB			MSB	0	0	0	Thermal Asperity Rate (TAR)
231	E7	LSB MSB	0	0	0	0	0	0	Controller Temperature
234	EA	LSB						MSB	Total Bytes Read from NAND Flash
235	EB	LSB						MSB	Total Host Bytes/Sectors Written to Device
241	F1	LSB						MSB	Total Nand Bytes/Sectors Written to NAND Flash
242	F2	LSB						MSB	Total Bytes Read from Device (32MB/unit)
248	F8	LSB MSB	0	0	0	0	0	0	Remaining Life %
249	F9	LSB MSB	0	0	0	0	0	0	Spare Block Remaining

4.4 SMART Command Transport

Table 4-6

Action Code (hex)	Description
0003h	Error recovery control (the time needed to recover)
0004h	Features control
0005h	SCT data tables

4.5 Set Features

Table 4-7

Value (hex)	Description
2	Enable write cache
66	Disable reverting to Power-On defaults
82	Disable write cache
CC	Enable reverting to Power-On defaults

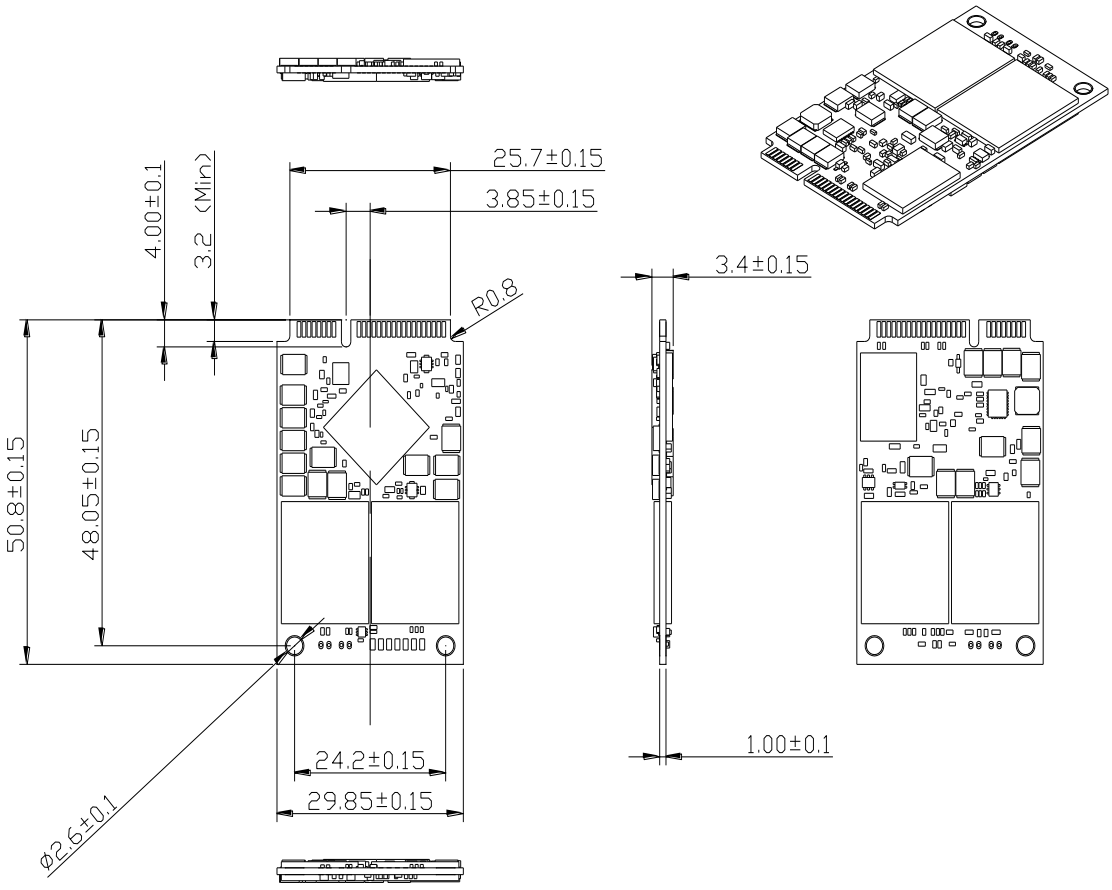
5.0 Mechanical Information

5.1 Physical Dimension Specifications

Table 5-1

Type		Value
mSATA	Length	50.80 mm +/- 0.15mm
	Width	29.85 mm +/- 0.15 mm
	Thickness	3.40 mm +/- 0.15mm

5.2 Mechanical Form Factor (Units in mm)



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